YAMAHA LSI

YMZ284

Software-controlled Sound Generator (SSGL)

■ OVERVIEW

The YMZ284(SSGL) is a melody and effect sound generator LSI, having square wave, noise and envelope generators.

The YMZ284 is packaged in 16-pin DIP with easy control, eliminating the I/O port and improving CPU interface from the YM2149 (SSG).

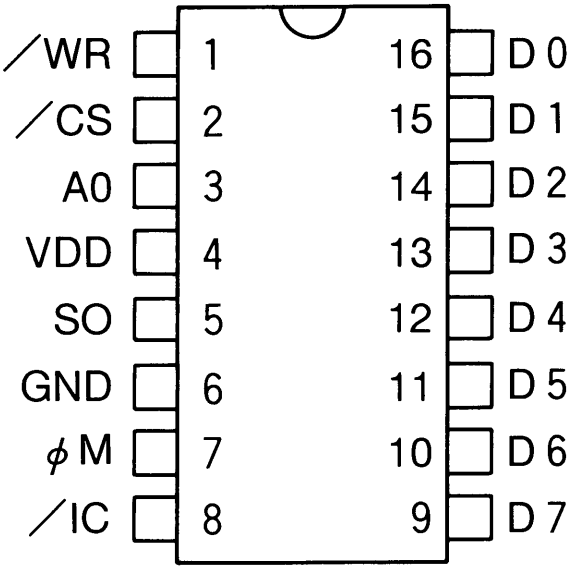
■ FEATURES

- Three sequence square wave generators and one noise generator, software-compatible with the YM2149(SSG)
- 3 built-in 5-bit D/A convertors and mixed output
- CPU interface through ／CS, ／WR control signal and 8 bit data bus
- Wide voicing range of 8 octaves
- Smooth attenuation by wide dynamic range envelope generator
- Power down mode
- +5V single power supply, silicon gate CMOS process
- 16-pin plastic DIP(YMZ284-D) or 16-pin plastic SOP (YMZ284-M).

YAMAHA CORPORATION

YMZ284 CATALOG
CATALOG No. : -LSI 4MZ2843
1994. 11

■ PIN OUT DIAGRAM



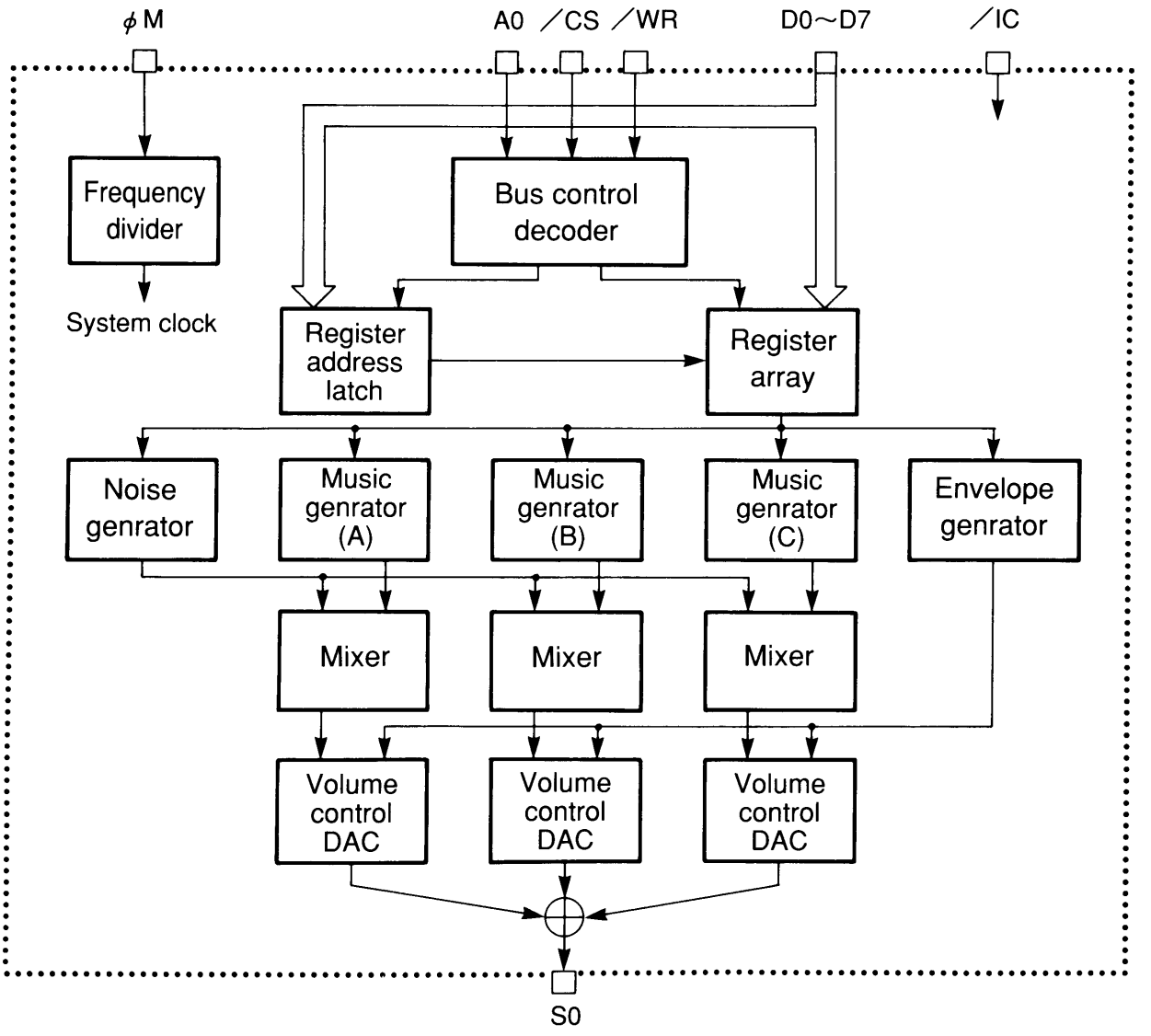
Top View (16pin DIP, 16pin SOP)

■ PIN DESCRIPTION

No	Name	I/O	Function
1	/WR	I	CPU interface Write enable
2	/CS	I	CPU interface Chip select
3	A 0	I	CPU interface Address/Data select
4	VDD	–	+5V power supply
5	SO	O	D/A convertor output for SSG
6	GND	–	Ground
7	φM	I	Master clock input
8	/IC	I+	Initial clear input
9	D 7	I	CPU interface data bus (MSB)
10	D 6	I	CPU interface data bus
11	D 5	I	CPU interface data bus
12	D 4	I	CPU interface data bus
13	D 3	I	CPU interface data bus
14	D 2	I	CPU interface data bus
15	D 1	I	CPU interface data bus
16	D 0	I	CPU interface data bus (LSB)

Note) I+ : Built-in pull-up registor

■BLOCK DIAGRAM



■FUNCTIONS

1. φM

Master clock input pin.

Frequency is 1MHz to 4MHz.

2. D0～D7

8 bit data bus.

3. /CS・/WR・A0

Control write address and data from 8 bit data bus.

/CS	/WR	A0	Function
L	L	L	Address write mode
L	L	H	Data write mode

4. /IC

'L' level resets the system clearing all register values.

5. SO

Analog output pin

6. VDD

+5V power supply pin

7. GND

Ground pin

■FUNCTION DESCRIPTION

All functions of SSGL are controlled by the 15 internal registers.

Music generator .....Generates square waves of a different frequencies for each channel (A, B, and C).
Noise generator.....Generates pseudo-random waveforms (variable frequency).
Mixer.....Mixes 3-channels (A, B, and C) music and 1-channel noise generator output.
Volume control .....Constant level or variable level is given for each of the three channels (A, B, and C).
Constant levels are controlled by the CPU, and variable levels by the envelope generator.
Envelope generator .....Generates various types of attenuation.
D/A convertor .....Outputs mixed analog signal.

■REGISTER ARRAY

ADDR	Function	D7	D6	D5	D4	D3	D2	D1	D0
$00	Channel A frequency	8 bit fine tone adjustment							
$01						4 bit rough tone adjustment			
$02	Channel B frequency	8 bit fine tone adjustment							
$03						4 bit rough tone adjustment			
$04	Channel C frequency	8 bit fine tone adjustment							
$05						4 bit rough tone adjustment			
$06	Noise frequency				5 bit noise frequency				
$07	Mixer setting			Noise			Tone		
				C	B	A	C	B	A
$08	Channel A level				M	L3	L2	L1	L0
$09	Channel B level				M	L3	L2	L1	L0
$0A	Channel C level				M	L3	L2	L1	L0
$0B	Envelope frequency	8 bit fine adjustment							
$0C		8 bit rough adjustment							
$0D	Envelope shape					CONT	ATT	ALT	HOLD
$0F	Control power	'0'	'0'	'0'	'0'				

Note) 1 : D7, D6, D5, and D4 bit of register $0F must be '0'.

■REGISTER FUNCTION

● Music frequency setting ($00~$05)

The frequency f_T of the square wave generated by each music generator (A, B, and C) is calculated by the following equation.

$$f_T = \frac{f_{Master}}{32TP}$$

	D7	D6	D5	D4	D3	D2	D1	D0
$00 (CH-A) $02 (CH-B) $04 (CH-C)	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0

	D7	D6	D5	D4	D3	D2	D1	D0
$01 (CH-A) $03 (CH-B) $05 (CH-C)					TP11	TP10	TP9	TP8

f_{Master} is the frequency of master clock.

$TP=TP11*2^{11}+TP10*2^{10}+TP9*2^{9}+TP8*2^{8}+TP7*2^{7}+TP6*2^{6}+TP5*2^{5}+TP4*2^{4}+TP3*2^{3}+TP2*2^{2}+TP1*2+TP0$

● Noise generator setting ($06)

The noise frequency f_N is calculated by the following equation.

$$f_N = \frac{f_{Master}}{32NP}$$

	D7	D6	D5	D4	D3	D2	D1	D0
$06				NP4	NP3	NP2	NP1	NP0

f_{Master} is the frequency of the master clock.

$NP=NP4*2^{4}+NP3*2^{3}+NP2*2^{2}+NP1*2+NP0$

● Mixer setting ($07)

Setting '0' enables sound output.
Mixed sound is output when both Noise and Tone outputs are set for the same channel.

	D7	D6	D5	D4	D3	D2	D1	D0
$07			Noise			Tone		
			C	B	A	C	B	A

● Volume control and D/A convertor ($08~$0A)

The audio output level from the D/A convertors for the three channels (A, B, and C) is controlled as follows.

	D7	D6	D5	D4	D3	D2	D1	D0
$08 (CH-A) $09 (CH-B) $0A (CH-C)				M	L3	L2	L1	L0

When M=0, the output level is determined by the 4 bits of L3, L2, L1 and L0.

When M=1, the output level is determined by the 5 bits of E4, E3, E2, E1 and E0 of the envelope generator of the SSGL. (This output level is variable as E4~E0 change over time.)

When the maximum amplitude of the 5-bit D/A convertor is normalized to 1V, the output levels shown in Fig.1 are obtained.

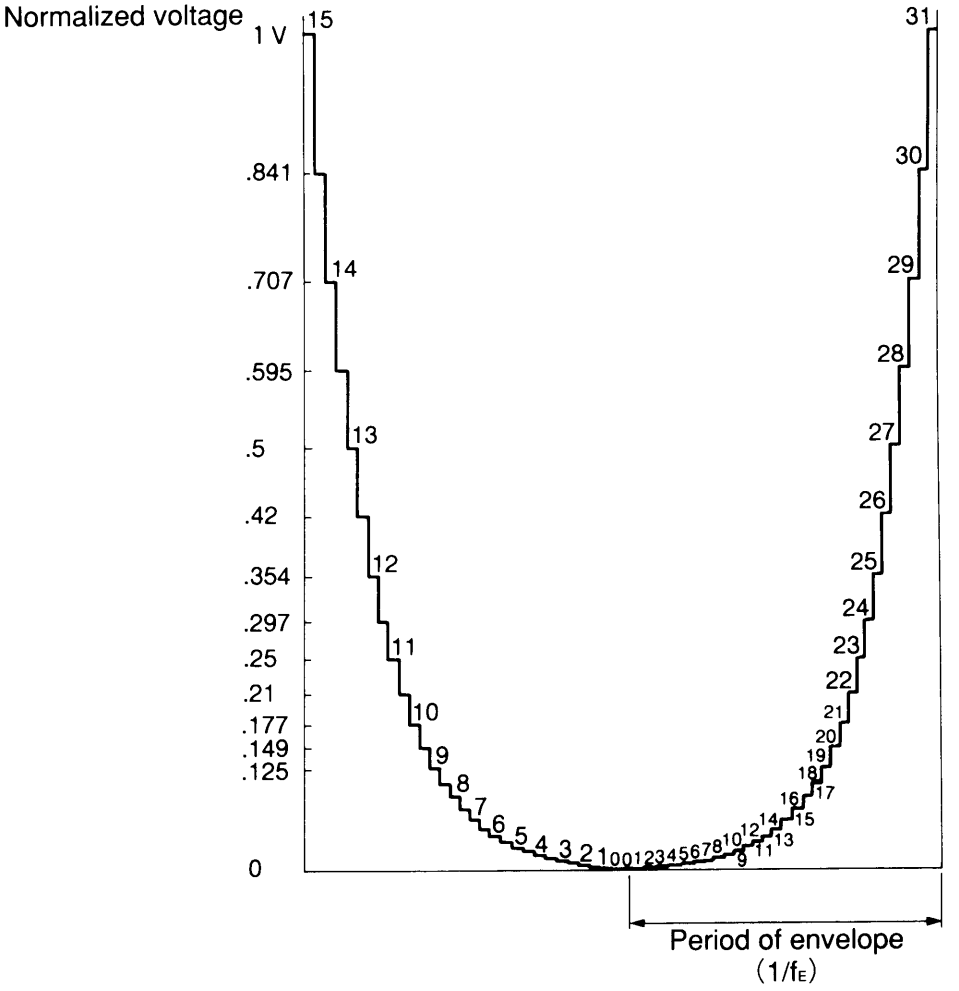


Fig.1 Output level of D/A convertor

The left half of the diagram shows fixed levels set by L3, L2, L1 and L0 bits.

The right half of the diagram shows output levels set by E4, E3, E2, E1 and E0 bits.

● Envelope frequency setting ($0B~$0C)

The envelope repetition frequency f_E is calculated by the following equation.

	D7	D6	D5	D4	D3	D2	D1	D0
$0B	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0

	D7	D6	D5	D4	D3	D2	D1	D0
$0C	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8

$$f_E = \frac{f_{Master}}{512EP}$$

f_{Master} is the frequency of the master clock.

$EP=EP15*2^{15}+EP14*2^{14}+EP13*2^{13}+EP12*2^{12}+EP11*2^{11}+EP10*2^{10}+EP9*2^{9}+EP8*2^{8}+EP7*2^{7}+EP6*2^{6}+EP5*2^{5}+EP4*2^{4}+EP3*2^{3}+EP2*2^{2}+EP1*2+EP0$

The period of the actual frequency f_{EA} used for the nvelope generated is 1/32 of the envelope repetition period ($1/f_E$).

● Envelope shape control ($0D)

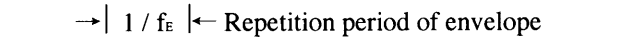
The envelope generator counts the envelope clock f_{EA} 32 times for each envelope pattern cycle. The envelope level is determined by the 5 bit output (E4~E0) of the counter.

	D7	D6	D5	D4	D3	D2	D1	D0
$0D					CONT	ATT	ALT	HOLD

The shape of this envelope is created by increasing, decreasing, stopping, or repeating this counter.

Below envelope types are selected by CONT, ATT, ALT and HOLD setting.

D_3	D_2	D_1	D_0	Envelope shape
CONT	ATT	ALT	HOLD	
0	0	×	×	
0	1	×	×	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	



■ELECTRICAL CHARACTERISTICS

1. Absolute maximum ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 ~ 7.0	V
Input voltage	V_I	V_{SS}−0.3 ~ V_{DD}+0.3	V
Storage temperature	T_{stg}	−50 ~ 125	°C

2. Recommended operating conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.75	5	5.25	V
Operation temperature	T_{OP}	0	25	70	°C

3. DC Characteristics (Conditions : Ta = 0~70 ℃, V_{DD} = 5.0±0.25V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input highlevel voltage	V_{IH}	*1	2.2			V
Input lowlevel voltage	V_{IL}	*1			0.8	V
Input highlevel voltage	V_{IH}	*2	3.5			V
Input lowlevel voltage	V_{IL}	*2			1.0	V
Input leak current	I_{LI}	V_I = 0~5V, *1	−10		10	μA
Pull-up registance	R_U	*2	60	250	600	kΩ
Input capacity	C_I	*3			10	pF
Power supply current	I_{DD}				10	mA

Note) *1 : Applied to all input pins except /IC.
*2 : Applied to /IC.
*3 : Applied to all input pins.

4. Analog Characteristics (Conditions : Ta=0~70℃, V_{DD}=5.0±0.25V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog output voltage	V_{OA}	*1	1.50	1.70	1.90	V

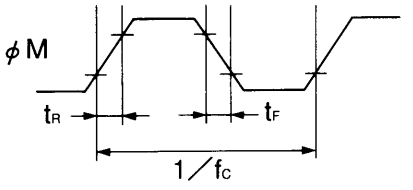
Note) *1 : Applied to SO pin. Maximum volume, R_L=1kΩ, peak to peak.

5. AC Characteristics (Conditions : Ta = 0~70℃, V_{DD} = 5.0±0.25V)

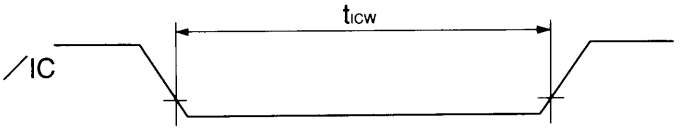
Item	Symbol	Min.	Typ.	Max.	Unit
Master clock frequency	f_C	1		4	MHz
Master clock duty	D	40		60	%
Master clock rise time	t_R			20	ns
Master clock fall time	t_F			20	ns
Reset pulse width	t_{ICW}	5			μs
Address setup time	t_{AS}	20			ns
Address hold time	t_{AH}	10			ns
Chip select write width	t_{CSW}	30			ns
Write pulse write width	t_{WS}	0			ns
Write data hold time	t_{WH}	0			ns
Write data setup time (Address)	t_{WDSA}	10			ns
Write data setup time (Data)	t_{WDSD}	10			ns
Write data hold time (Address)	t_{WDHA}	10			ns
Write data hold time (Data)	t_{WDHD}	10			ns

6. Timing diagram

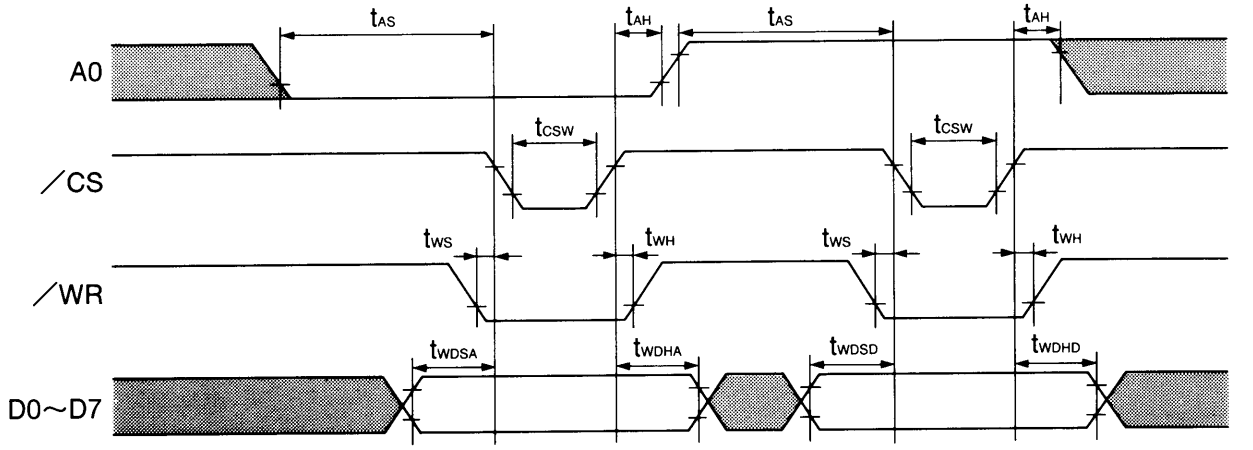
(1) Master clock timing



(2) Reset timing

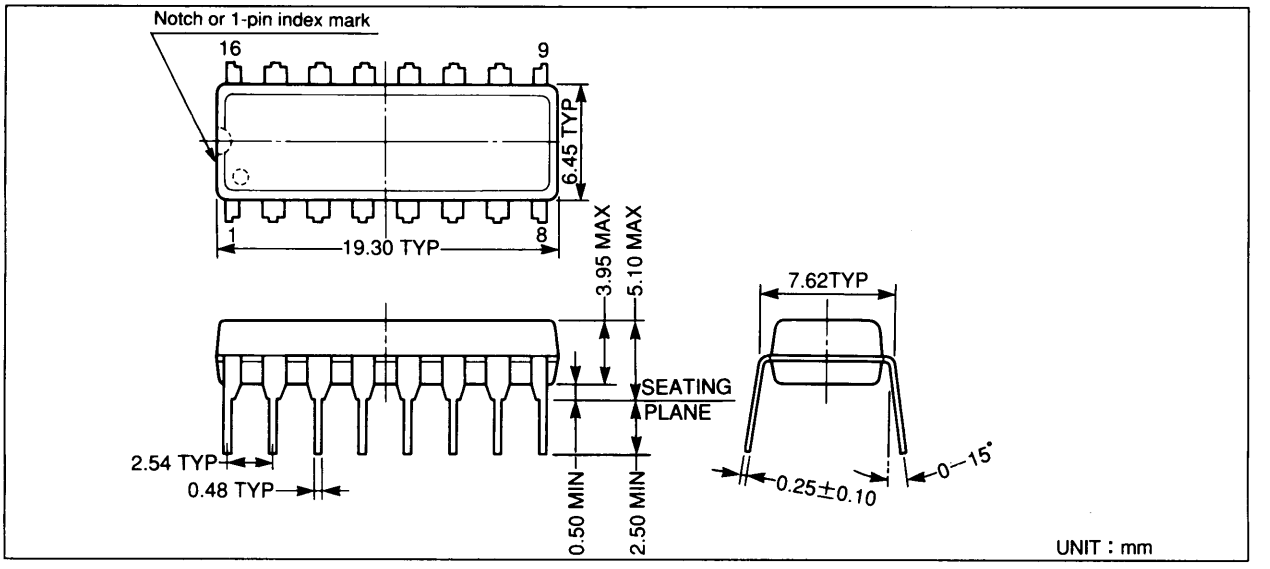


(3) CPU interface timing

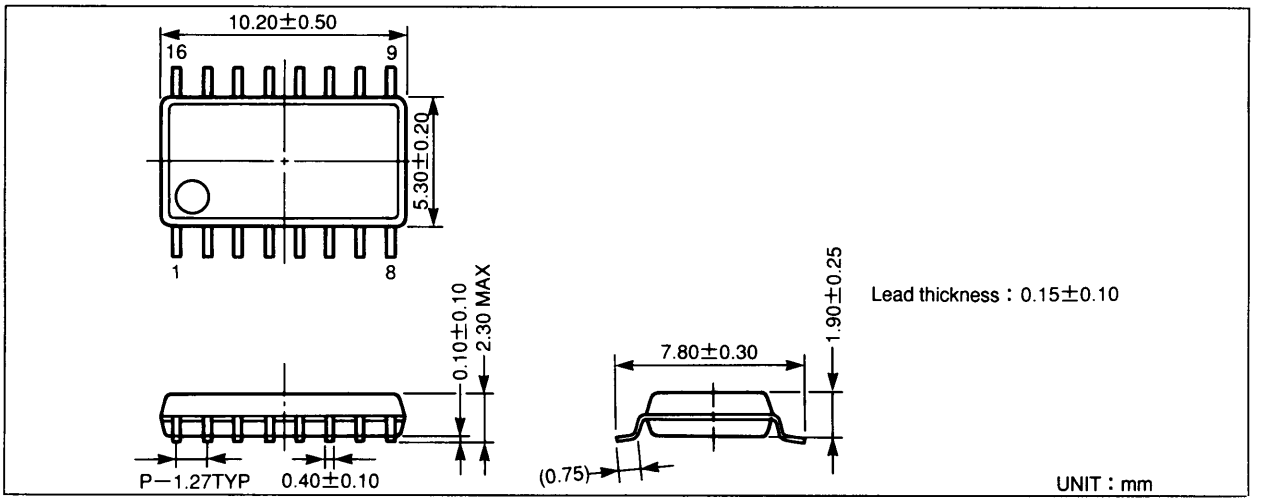


■ EXTERNAL DIMENSIONS

● YMZ284-D



● YMZ284-M



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